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(54) Method of manufacturing gate insulated field effect transistors.

(57) A method of manufacturing thin film field effect transistors is described. The channel region of the transistor is formed by depositing an amorphous semiconductor film followed by thermal treatment for converting the amorphous phase to a polycrystalline phase. The deposition of the amorphous semiconductor film is carried out by sputtering in an atmosphere comprising hydrogen in order to introduce hydrogen into the amorphous semiconductor film, and a gate insulating oxide film is deposited by sputtering in an atmosphere comprising oxygen. The method enables field effect transistors to be formed on large area substrates and is particularly useful in the manufacture of liquid crystal display panels.

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of manufacturing semiconductor devices and, more particularly to a method of manufacturing thin film gate insulated field effect transistors comprising polycrystalline semiconductor films.

2. Description of the Prior Art

The prior art includes methods utilizing low pressure CVD for the deposition of polycrystalline semiconductor thin films at temperatures ranging from 550° C to 900° C. Recently, with the development of liquid crystal panels having wide display areas, the need has arisen for a deposition technique which will enable polycrystalline semiconductor films to be provided over large area substrates.

Polycrystalline films are formed by depositing amorphous semiconductor films by low pressure CVD and then recrystallizing the amorphous films, since direct deposition of polycrystalline films over wide areas is difficult for the reason of reaction temperature. Furthermore, it is very difficult to deposit uniform semiconductor films by low pressure CVD. Problems also arise with plasma CVD which requires long deposition times.

Sputtering on the other hand is excellent in this sense. In particular, there are the following advantages when films are deposited by magnetron sputtering:

1) The surfaces of substrates are less damaged by high energy electrons since the electrons are confined to the vicinity of the target;

2) Wide areas can be coated at lower temperatures; and

3) No dangerous gas is used so that safe and practicable processes are ensured.

The sputtering is conventionally carried out without hydrogen because the electric characteristics of hydrogenated amorphous semiconductors deposited by sputtering are not so good as to satisfy the requirements of channel formation for transistors. Semiconductor films deposited by sputtering, however, have a disadvantage that thermal crystallization thereof is very difficult.

OBJECTS AND SUMMARY OF THE INVENTION

It is thus an object of the present invention to provide a method of manufacturing gate insulated field effect transistors comprising polycrystalline semiconductor films over a wide substrate area.

To achieve the foregoing and other objects the present invention proposes that a semiconductor film intended to form a channel region is deposited by sputtering in an atmosphere comprising hydrogen, and/or that an oxide film intended to form a gate insulating region is deposited by sputtering in an atmosphere comprising oxygen.

In accordance with a preferred embodiment of the present invention, the semiconductor film is deposited in an amorphous phase or an equivalent phase. The amorphous semiconductor is then subjected to thermal treatment at 450° C to 750° C, typically at 600° C, in order to convert the amorphous phase to a polycrystalline phase. This recrystallization takes place easily as compared to the conventional case abovementioned where no hydrogen is introduced. The reason for this is considered to be as explained in the following. In the conventional case, amorphous semiconductors such as a-Si are deposited and form a certain type of microstructure in which the distribution of silicon atoms is uneven. This micro-structure hinders the Progress of recrystallization. The inventors of the present invention have confirmed that the formation of such a microstructure is prevented by introducing hydrogen into the semiconductor film, so that the resulting film can be easily recrystallized by thermal treatment. The average diameter of polycrystals formed after the thermal treatment is of the order of 5Å to 400Å. The proportion of hydrogen introduced into the film may be no higher than 5 atom%, but may be between 5 and 100 atom %.

Another important feature of the semiconductor film produced in accordance with the present invention is lattice distortion which enables close connection between polycrystals at interfaces thereof, and the method of the present invention enables films which possess lattice distortion to be obtained. This feature helps to cancel out the formation of barriers at the crystal interfaces, whereas in the absence of such lattice distortions, impurity atoms such as oxygen tend to collect at the interfaces so forming crystal barriers which hinder transportation of carriers. Because of this, the mobility (field mobility) of electrons in the semiconductor film formed in accordance with the present invention is improved to as high as 5 to 300 $cm^2/V \cdot S$. The present invention thus provides an impurity-proof manufacturing method. Even in the case of relatively many oxygen atoms occurring in the semiconductor film, the manufacturing method of the present invention can still produce acceptable

transistors.

Furthermore, semiconductor film deposited by sputtering in accordance with the invention is so fine and dense as not to allow oxidation to reach to the inside of the film and only very thin oxide films are formed at the surface thereof, whereas semiconductor film deposited by plasma CVD includes a relatively high proportion of its amorphous phase which enables oxidation to progress into the inside of the semiconductor. This fine structure of the present invention helps to reduce interfacial barriers between crystals in association with lattice distortion.

The atmosphere in which sputtering for deposition of the semiconductor film is carried out may be hydrogen, a mixture of hydrogen and an inert gas such as Ar and/or He, or a hydrogen compound which does not change the property of the semiconductor film such as SiH_4 or Si_2H_6. The existence of hydrogen in the sputtering atmosphere plays an important role in obtaining a semiconductor film having sufficient lattice distortions therein. In the case of hydrogen/argon mixtures, the hydrogen proportion may be selected to be between 5% and 100% (therefore the argon proportion is between 95% and 0%), and typically is between 25% and 95% (argon between 75% and 5%).

The gate insulating film may be deposited in the same manner as the deposition of the semiconductor film except that the sputtering atmosphere is replaced by an oxidizing atmosphere. By virtue of this replacement, an oxide film can be formed by sputtering.

The above and other features of the present invention are set forth with particularity in the appended claims and will be well understood from consideration of the following detailed description given with reference to the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

Fig.1(A) is a schematic view showing a Planar type magnetron RF sputtering apparatus suitable for use in manufacturing thin film field effect semiconductor transistors in accordance with the present invention;

Fig.1 (B) is an explanatory view showing the arrangement of magnets provided in the apparatus illustrated in Fig.1(A);

Figs. 2(A) to 2(E) are cross-sectional views showing a method of manufacturing thin film field effect semiconductor transistors in accordance with a first embodiment of the present invention;

Fig.3 (A) is a graphical diagram showing the relationship between the partial pressure of hydrogen in the atmosphere in which semiconductor films are deposited and the field mobility of the semiconductor film;

Fig.3 (B) is a graphical diagram showing the relationship between the partial Pressure of hydrogen in the atmosphere in which semiconductor films are deposited and the threshold voltage of the transistor consisting of the semiconductor film;

Figs.4 to 8 are graphical diagrams showing the relationships between the drain current and the drain voltage of field effect transistors manufactured in accordance with the present invention;

Fig.9 is a graphical diagram showing Raman spectra of semiconductor films deposited under several deposition conditions; and

Figs.10(A) and 10(B) are cross-sectional views showing thin film field effect semiconductor transistors formed in accordance with second and third embodiments of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Referring to Fig.1 (A) , a planar type magnetron RF sputtering apparatus suitable for use in manufacturing thin film field effect semiconductor transistors in accordance with the present invention is illustrated. The apparatus comprises a vacuum chamber 1, an evacuation system 2 consisting of a turbo molecular pump 2b and a rotary pump 2d respectively provided with valves 2a and 2c, a metallic holder 3 fixed in the lower side of the chamber 1 for supporting a target 4 thereon, the holder being formed with an inner conduit 3a through which a coolant can flow to cool the target 4 and being provided with a number of magnets 3b, an energy supply 5 consisting of an RF (e.g. 13.56MHz) source 5a provided with a matching box 5b for supply RF energy to the holder 3, a substrate holder 6 located in the upper side of the chamber 1 for supporting a substrate 11 to be coated, a heater 6a embedded in the substrate holder 6, a shutter 7 between the substrate 11 and the target 4 and a gas feeding system 8. Numeral 9 designates sealing means for ensuring the air-tight structure of the vacuum chamber 1. In advance of actual deposition on the substrate 11, impurities occurring in the targets are sputtered and deposited on the shutter 7 between the substrate 11 and the target 4, and then the shutter is removed in order to enable normal deposition on the substrate 11. The magnets 3b are oriented to have their N poles at their upper ends (as viewed in the figure) and S poles at their lower ends, and are horizontally arranged in a circle as illustrated in Fig.1 (B) in order to confine electrons in a sputtering region between the

substrate 11 and the target 4.

Referring now to Figs.2(A) to 2(E), a method of manufacturing thin film field effect transistors in accordance with a first preferred embodiment of the invention will be described.

A glass substrate 11 is disposed in the magnetron RF sputtering apparatus shown in Figs.1(A) and 1 (B) and is coated with a SiO_2 film 12 to a thickness of 200nm in a 100% O_2 atmosphere (0.5 Pa) at a substrate temperature of 150°C. The output power of the apparatus is 400W in terms of 13.56 MHz RF energy. Single crystalline silicon is used as a target. An amorphous silicon film is then deposited in the sputtering apparatus on the SiO_2 film 12 to a thickness of 100nm. The atmosphere comprises a mixture consisting of hydrogen and argon so that $H_2/(H_2+Ar) = 0.8$ in terms of partial pressure. The total pressure is 0.5 Pa: the output power of the apparatus is 400W in terms of 13.56 MHz RF energy: single crystalline silicon is used as a target: and the substrate temperature is maintained at 150°C (deposition temperature) by the heater 6a. In preferred embodiments, the hydrogen proportion in the mixture is chosen between 5% and 100%; the deposition temperature between 50° C and 500° C; the output power between 100W and 10MW in a frequency range from 500Hz to 100GHz which may be combined with another pulse energy source.

The amorphous silicon film is then subjected to thermal treatment at 450° C to 700° C, typically at 600°C, for 10 hours in a hydrogen or an inert atmosphere, e.g. in 100% nitrogen. The film is recrystallized by this treatment. In accordance with experiments, it was confirmed by SIMS analysis that oxygen, carbon and hydrogen were involved respectively at densities of 2×10^{20}cm-3, $5 \times 10^{18}cm^{-3}$ and no higher than 5%. These density figures were minimum values for the respective elements and varied along the depth direction. The reason why minimum values were measured is that a natural oxide existed at the surface of the semiconductor film. These concentrations were not changed even after the recrystallization.

The impurities such as oxygen usually tend to be collected at interfaces between crystals and form interfacial barriers in the semiconductors. In the case of the semiconductor film formed according to the present invention, however, lattice distortion prevents the formation of barriers and therefore oxygen concentrations, even of the order of $2x10^{20}cm^{-3}$, exert little influence upon the transportation of carriers and cause no practical problems. The existence of lattice distortions was indicated by a shift in a laser Raman spectra peak towards the lower wave number direction as shown in Fig.9, which will be explained later.

The semiconductor film is next etched to produce a pattern necessary to form a number of transistors in the substrate 11 in accordance with the following procedure. The film 13 shown in Fig.2(A) corresponds to one of the transistors to be formed.

Next, an n^+- type amorphous silicon semiconductor film is deposited on the film 13 in the magnetron RF sputtering apparatus to a thickness of 50 nm. The atmosphere comprises a mixture consisting of H_2 at 10% to 99%, e.g. 80%, Ar at 10% to 90%, e.g. 19% and PH_3, at no higher than 10%, e.g. no higher than 1% in terms of partial pressure. The total pressure is 0.5 Pa: the output power of the apparatus is 400W in terms of 13.56 MHz RF energy: a single crystalline silicon is used as a target: and the substrate temperature in the apparatus is maintained at 150° C. The doping with phosphorus may be performed by any other suitable technique, such as ion implantation or the use of a target in which a phosphorus impurity has been doped in advance. Boron may be used instead of phosphorous as a dopant. The impurity semiconductor film is then patterned to form source and drain regions 14 as shown in Fig.2(B) .

The entire surface of the structure is then coated with a silicon oxide film to a thickness of 100 nm by magnetron RF sputtering as illustrated in Fig.2(C). The atmosphere comprises a high density oxygen diluted with an inert gas, preferably, 100% oxygen at 0.5 Pa: the output power of the apparatus is 400W in terms of 13.56 MHz Rf energy: a single crystalline silicon or an artificial quartz is used as a target: and the substrate temperature is maintained at 100° C. When pure oxygen (100% oxygen) is used as the atmosphere, the surface level density of the gate insulating film can be decreased so that excellent transistor characteristics are realized.

After opening contact holes in the oxide film 15 as shown in Fig.2(D), an aluminum film 16 is deposited by vapor evaporation to a thickness of 300 nm and patterned in order to form a gate electrode G and source and drain contact electrodes S and D. Finally, the entire structure is subjected to thermal annealing in a 100% hydrogen atmosphere at 375° C for 30 minutes. The hydrogen thermal annealing is carried out for the purpose of lowering interfacial potentials and improving device characteristics. As a result, a thin film transistor is formed with a channel region of 100μm x 100μm. The properties of the transistor have been examined as will be described hereinafter.

The above procedure was repeated under different deposition conditions for the semiconductor film 12. The proportion of hydrogen in the hydrogen/Ar mixture atmosphere was changed to be $H_2/(H_2+Ar) = 0$, 0.05, 0.2, 0.3, 0.5 and 0.8 respectively in term of partial pressure. Fig.3 (A) is a graphical diagram showing the field mobility versus the proportion of hydrogen ($P_M/P_{TOTAL}=H_2/(H_2+Ar)$). In accordance with this diagram, high values of the field mobility can be attained if the hydrogen proportion is no lower than 20%. Fig.3 (B) is a graphical diagram showing the threshold voltage versus the hydrogen proportion. As shown from this diagram, field

effect transistors of normally off type can be formed to have threshold voltages of no higher than 8V, which is desirable from a practical view point, if the hydrogen proportion is no lower than that of argon. This means that transistors having good characteristics can be formed by fabricating channel regions by depositing amorphous silicon film through sputtering carried out in a hydrogen atmosphere and subjecting the film to thermal treatment. The electric characteristics tend to be improved as the hydrogen proportion is increased.

Figs.4 to 8 are graphical diagrams showing the relationship between the drain current and the drain voltage. The proportion of hydrogen of the hydrogen/Ar mixture atmosphere, i.e. $H_2/(H_2+Ar)$, were 0 (Fig.4), 0.05 (Fig.5), 0.2 (Fig.6). 0.3 (Fig.7) and 0.5 (Fig.8) respectively in term of partial pressure. Curves 41, 51, 61, 71, and 81 correspond to the case in which measurement was effected with the application of 20 V at the gate electrode. Curves 42, 52, 62, 72 and 82 correspond to the case in which measurement was effected with the gate electrode at 25 V. Curves 43, 53, 63, 73 and 83 correspond to the case in which measurement was effected with the gate electrode at 30 V. The conspicuous effect of the present invention is apparent when Fig.5 is compared with Fig.6. Namely, when curve 53 is compared to curve 63, it can be seen that the drain current in the case of the hydrogen proportion being 0.2 was larger than that when the hydrogen proportion was 0.05 by a factor of 10 or more. This means that the characteristics of transistors are significantly improved when the proportion of hydrogen in the atmosphere in which the amorphous silicon film 13 is deposited is increased from 5% to 20%. This is confirmed also by the following experiments.

The proportion of hydrogen of the hydrogen/Ar mixture atmosphere in which the channel region was deposited was changed to be $H_2/(H_2+Ar)$ = 0, 0.05, 0.2, 0.3 and 0.5 respectively in term of partial pressure. Fig.9 is a graphical diagram showing Raman spectra of the semiconductor film 12 after the thermal treatment. The proportions of hydrogen of the hydrogen/Ar mixture atmosphere, i.e. $H_2/(H_2+Ar)$, were 0 (curve 91), 0.05 (92), 0.2 (curve 93) and 0.5 (curve 94) respectively in term of partial pressure. As shown in the diagram, the crystallinity was conspicuously enhanced when the hydrogen proportion was increased to 20% (curve 93) as compared with the case of 5% (curve 92). The average diameter of constituent crystals of the film in the case of 20% was 5Å to 400Å, typically 50Å to 300Å. The peak position of the Raman spectra was shifted to the small wave number direction by an amount Δ (approx. 10 cm^{-1}) with reference to the peak position for single crystalline silicon, i.e. 522cm^{-1}, and this shift indicates lattice distortion. The film is dense and therefore crystals thereof are contracted. Because of the contraction and the lattice distortion each crystal can be more closely connected with its neighbours and fewer impurities are collected at the interfaces, lowering the barrier height. As a result, high carrier mobilities can be realized even if the concentration of impurity in the film is as high as $2 \times 10^{20} cm^{-3}$.

Referring to Figs. 6, 7 and 8 again, it will be understood that the drain current increases as the hydrogen proportion increases by comparing curves 63, 73 and 83 with each other. The drain current ID is expressed by the following equation when the drain voltage VD is low (Solid State Electronics, vol.24, No.11, p.1059, 1981, printed in Britain).

$$ID = (W/L)\mu C(VG-VT)VD$$

In the above equation, W is the channel width of the transistor; L is the channel length; μ is the carrier mobility; C is the static capacity of the gate insulating oxide film; VG is the gate voltage; and VT is the threshold voltage, Curves plotted in Figs. 4 to 8 can be expressed by the equation in the vicinity of the origin. The carrier mobility μ and the threshold voltage VT are determined by giving the hydrogen proportion in the atmosphere whereas the values W, L and C are determined by the geometric design of the transistor. Accordingly, the variables of the equation are ID, VG and VD. Since, in Figs.4 to 8, curves are plotted with the variable VG being fixed, they are considered as two-variable functions expressed by the equation in the vicinity of the origin. The equation suggests that the gradient of each curve plotted in Figs.4 to 8 near the origin increases as the threshold voltage VT decreases and the mobility μ increases. This is apparent when comparing Figs.4 to 8 to each other with reference to the VT and μ of the respective cases which are shown in Figs.2 and 3. The equation also teaches the dependency of electric characteristics of the thin film transistor upon the VT and μ so that the device characteristics can not be determined only by one of Figs.2 and 3. when the gradients near origin of the respective curves plotted in Figs.4 to 8 are compared with each other for this reason, it is concluded that the hydrogen proportion should be not smaller than 20 %, preferably 100%.

This can be understood from the following consideration. Comparing Figs.4 to 8 with each other, the drain current increases as the hydrogen proportion increases toward 100% when the amorphous silicon film 13 is deposited by sputtering. This is apparent when comparing curves 43, 53, 63, 73 and 83.

The following is data showing the effects of the present invention:

H_2 proportion	S	VT	μ	on/off ratio
0	3.1	17.5	0.30	5.4
5	2.8	15.4	0.46	5.7
20	2.4	12.6	3.41	6.7
30	2.0	11.4	8.39	6.9
50	1.7	8.7	6.76	6.9
80	0.97	5.8	5.04	6.2

In the above data, H_2 proportion is the hydrogen proportion as discussed supra. S is the minimum value of $[d(ID)/d(VG)]^{-1}$ of the drain current ID as a function of the gate voltage VG in the vicinity of origin. A smaller S indicates sharper rise of the ID-VG function and better electric characteristics of the transistor. VT is the threshold voltage. The "μ" is the carrier mobility in units of $cm^2/V{\cdot}s$. The "on/off ratio" is the logarithm of the ratio of the drain current ID with VG being at 30V to the minimum value of the drain current ID when the drain voltage is fixed at 10V. From the data, it can be understood that it is preferred to choose a proportion of hydrogen in the sputtering atmosphere of 80% or more.

Referring now to Fig.10(A), a thin film field effect transistor in accordance with a second preferred embodiment of the present invention will be described. The deposition, the patterning and the thermal treatment of the insulating film 12 and the amorphous silicon film 13 are carried out in the same manner as the first embodiment. The entire structure is then coated with a 100nm thick silicon oxide film 15 by sputtering in an oxide atmosphere as described above. On the silicon oxide film 15 is deposited a polysilicon film which is highly doped with phosphorus followed by photolithography with a suitable mask in order to form a gate electrode 20.

With the gate electrode 20 or the mask used for forming it as a mask, self-aligned impurity regions, i.e. a source and a drain region 14 and 14' are formed by ion implantation. The intermediate region 17 of the silicon semiconductor film 13 between the impurity regions 14 and 14' is then defined as a channel region. Then, a thermal treatment may be carried out at 100° C to 500° C, for example 300° C, for 0.5 hour to 3 hours, for example 1 hour, in H_2 atmosphere in order to effect a thermal annealing. In this case, the interface state density is not more than 2×10^{11} cm^{-3}. An interlayer insulating film is coated over the entire surface of the structure followed by etching for opening contact holes in the interlayer film and the oxide film 15 in order to provide access to the underlying source and drain regions 14 and 14'. Finally, an aluminum film is deposited on the structure over the contact holes and patterned to form source and drain electrodes 16 and 16'. In accordance with this embodiment, since the source and drain regions and the channel region are formed in the same semiconductor film therefore the process can be simplified and the carrier mobility in the source and drain regions is improved because of the crystallinity of the semiconductor film 13.

Referring to Fig.10(B), a thin film field effect transistor in accordance with a third preferred embodiment of the present invention will be described. The deposition of the insulating film 12 is carried out in the same manner as the first embodiment. Next, however, a gate electrode 20 is formed by depositing and patterning a molybdenum film of a thickness of 3000Å as opposed to the case of the first embodiment.

The entire surface of the structure is then coated with a silicon oxide film 15 to a thickness of 100nm by magnetron RF sputtering. The atmosphere comprises a high density oxygen diluted with an inert gas, preferably, 100% oxygen at 0.5 Pa: the output power of the apparatus is 400W in terms of 13.56 MHz RF energy: a single crystalline silicon or an artificial quartz is used as a target: and the substrate temperature is maintained at 100°C. When pure oxygen (100% oxygen) is used as the atmosphere, the surface level density of the gate insulating film can be decreased so that excellent transistor characteristics are realized.

An amorphous silicon film is deposited in the sputtering apparatus on the silicon oxide film 15 to a thickness of 100 nm. The atmosphere comprises a mixture consisting of hydrogen and argon so that $H_2/(H_2+Ar) = 0.8$ in terms of partial pressure. The total pressure is 0.5 Pa: the output power of the apparatus is 400w in terms of 13.56 MHz RF energy: a single crystalline silicon is used as a target: and the substrate temperature is maintained at 150°C in the same manner. The amorphous silicon film is then given thermal treatment at 450° C to 700° C, typically at 600° C for 10 hours in a hydrogen or an inert atmosphere, e.g. in 100% nitrogen. The film is recrystallized by this treatment to be polycrystalline. In accordance with experiments, it was confirmed by SIMS analysis that oxygen, carbon and hydrogen atoms were involved respective at $1 \times 10^{20} cm^{-3}$, $4 \times 10^{18} cm^{-3}$ and no higher than 5%. These figures of density were minimum values of the respective elements which varied along the depth direction. Thus, a channel region 17 is formed on the gate electrode 20 through the gate insulating film 15.

Next, an n^+- type amorphous silicon semiconductor film is deposited on the film 13 in the magnetron RF

sputtering apparatus to a thickness of 50nm. The atmosphere comprises a mixture consisting of H_2 at 10% to 99%, e.g. 80%, Ar at 10% to 90%, e.g. 20% in terms of partial pressure. The total pressure is 0.5 Pa: the output power of the apparatus is 400W in terms of 13.56 MHz RF energy: a single crystalline silicon doped with phosphorus is used as a target: and the temperature in the apparatus is maintained at 150° C. The entire surface of the structure is coated with an aluminum film. The aluminum film and the n+-type film are patterned to form source and drain regions 14 and 14' and source and drain electrodes 16 and 16'. A channel region 17 is defined just below a gap between the source and the drain regions 14 and 14'. The gap is filled with an insulator 21 for protecting the channel region 17.

In accordance with the third embodiment, since the gate insulating film 15 is formed in advance of the formation of the semiconductor film 13 forming the channel 17, the interface between the insulating film 15 and the channel 17 is readily thermal annealed so that the density of surface levels can be decreased.

The foregoing description of preferred embodiments has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and obviously many modifications and variations are possible in light of the above teaching. The embodiment was chosen in order to explain most clearly the principles of the invention and its practical application thereby to enable others in the art to utilize most effectively the invention in various embodiments and with various modifications as are suited to the particular use contemplated. Examples are as follows:

The present invention can be applied to transistors utilizing other types of semiconductors such as germanium or silicon/germanium (Si_xGe_{1-x}) semiconductors, in which case the thermal treatment can be done at temperatures approx. 100°C lower than those used in the above embodiments. The deposition of such semiconductor can be carried out by sputtering in a high energy hydrogen plasma caused by optical energy (shorter than 1000nm wavelength) or electron cyclotron resonance (ECR). In this case, positive ions can be effectively produced so that the formation of microstructure in the semiconductor film thus deposited is further prevented. Instead of gases including hydrogen molecules, some hydrogen compounds can be used as the sputtering atmosphere so long as they do not give rise to impurities in the semiconductor. For example, monosilane or disilane may be used for forming silicon semiconductor transistors. And halogen such as helium may be used. Field effect transistors in accordance with the present invention may be manufactured by either of the following two ways, namely an amorphous semiconductor film or a polycrystalline semiconductor film may be deposited by any method, for example sputtering or vapor deposition (e.g. chemical vapor deposition or physical vapor deposition), and an oxide insulating film (gate insulating film) may be deposited by sputtering in an atmosphere comprising oxygen, or alternatively a semiconductor film may be deposited by sputtering in an atmosphere comprising hydrogen and an oxide insulating film (gate insulating film) may be deposited by any method. The semiconductor film can be deposited at a high deposition rate by sputtering and sputtering is suitable for mass production.

Claims

1. A method of manufacturing field effect transistors comprising:

   depositing a semiconductor film on an insulating surface by sputtering in an atmosphere comprising hydrogen;

   depositing an oxide insulating film on said semiconductor film by sputtering in an atmosphere comprising oxygen;

   forming a gate electrode on said semiconductor film with said oxide film insulating said semiconductor film from said gate electrode in order to define a channel region in said semiconductor film just below said gate electrode; and

   forming source and drain semiconductor regions adjacent to said channel region.

2. The method of claim 1 wherein the step of forming source and drain regions is carried out in advance of the step of forming said gate electrode.

3. The method of claim 2 wherein said source and drain regions are formed by forming an impurity semiconductor pattern coated on said semiconductor film in advance of the step of depositing the oxide insulating film.

4. The method of claim 1 wherein said source and drain regions are formed by implanting ions into said semiconductor film with said gate electrode as a mask.

5. The method of any preceding claim wherein said atmosphere comprising hydrogen comprises a mixture of hydrogen and argon.

6. The method of claim 5 wherein the hydrogen proportion of said mixture is 5% to 100%.

7. The method of any preceding claim wherein said semiconductor film is a silicon semiconductor.

8. The method of any preceding claim further comprising subjecting said semiconductor film to thermal treatment.

9. The method of claim 8 wherein said semiconductor film is deposited in an amorphous phase and recrystallized by said thermal treatment.

10. A method of manufacturing field effect transistors comprising:
forming a gate electrode on an insulating surface;
depositing an oxide insulating film on said gate electrode by sputtering in an atmosphere comprising oxygen;
depositing a semiconductor film on said oxide insulating film by sputtering in an atmosphere comprising hydrogen to form a channel region in said semiconductor film just above said gate electrode; and
forming source and drain semiconductor regions adjacent to said channel region.

11. The method of claim 10 wherein said source and drain regions are formed by forming an impurity semiconductor patterned film coated on said semiconductor film except on said channel region.

12. The method of claim 10 or 11 wherein said atmosphere comprising hydrogen comprises a mixture of hydrogen and argon.

13. A method of manufacturing field effect transistors comprising:
depositing a semiconductor film on an insulating surface;
depositing an oxide insulating film on said semiconductor film by sputtering in an atmosphere comprising oxygen;
forming a gate electrode on said semiconductor film with said oxide film insulating said semiconductor film from said gate electrode in order to define a channel region in said semiconductor film just below said gate electrode; and
forming source and drain semiconductor regions adjacent to said channel region.

14. The method of claim 13 wherein said semiconductor film is deposited by vapor deposition.

15. The method of claim 13 wherein said semiconductor film is deposited by sputtering.

16. A method of manufacturing field effect transistors comprising:
forming a gate electrode on an insulating surface;
depositing an oxide insulating film on said gate electrode by sputtering in an atmosphere comprising oxygen;
depositing a semiconductor film on said oxide insulating film to form a channel region in said semiconductor film just above said gate electrode; and
forming source and drain semiconductor regions adjacent to said channel region.

17. The method of claim 16 wherein said semiconductor film is deposited by vapor deposition.

18. The method of claim 16 wherein said semiconductor film is deposited by sputtering.

19. A method of manufacturing field effect transistors comprising:
depositing a semiconductor film on an insulating surface by sputtering in an atmosphere comprising hydrogen;
depositing an oxide insulating film on said semiconductor film;
forming a gate electrode on said semiconductor film with said oxide film insulating said semiconductor film from said gate electrode in order to define a channel region in said semiconductor film just below

said gate electrode; and
forming source and drain semiconductor regions adjacent to said channel region.

20. The method of claim 19 further subjecting said semiconductor film to thermal treatment.

21. A method of manufacturing field effect transistors comprising:
forming a gate electrode on an insulating surface;
depositing an oxide insulating film on said gate electrode;
depositing a semiconductor film on said oxide insulating film by sputtering in an atmosphere comprising hydrogen to form a channel region in said semiconductor film just above said gate electrode; and
forming source and drain semiconductor regions adjacent to said channel region.

22. The method of claim 21 further comprising subjecting said semiconductor film to thermal treatment.

23. A method of manufacturing field effect transistors on large area substrates, said method including the formation of one or more transistor layers by sputtering and being characterized in that a semiconductor layer is formed by sputtering in an atmosphere comprising hydrogen.

24. A method of manufacturing field effect transistors on large area substrates, said method including the formation of one or more transistor layers by sputtering and being characterized in that an oxide insulating layer is formed by sputtering in an atmosphere comprising oxygen.

FIG. 1(A)

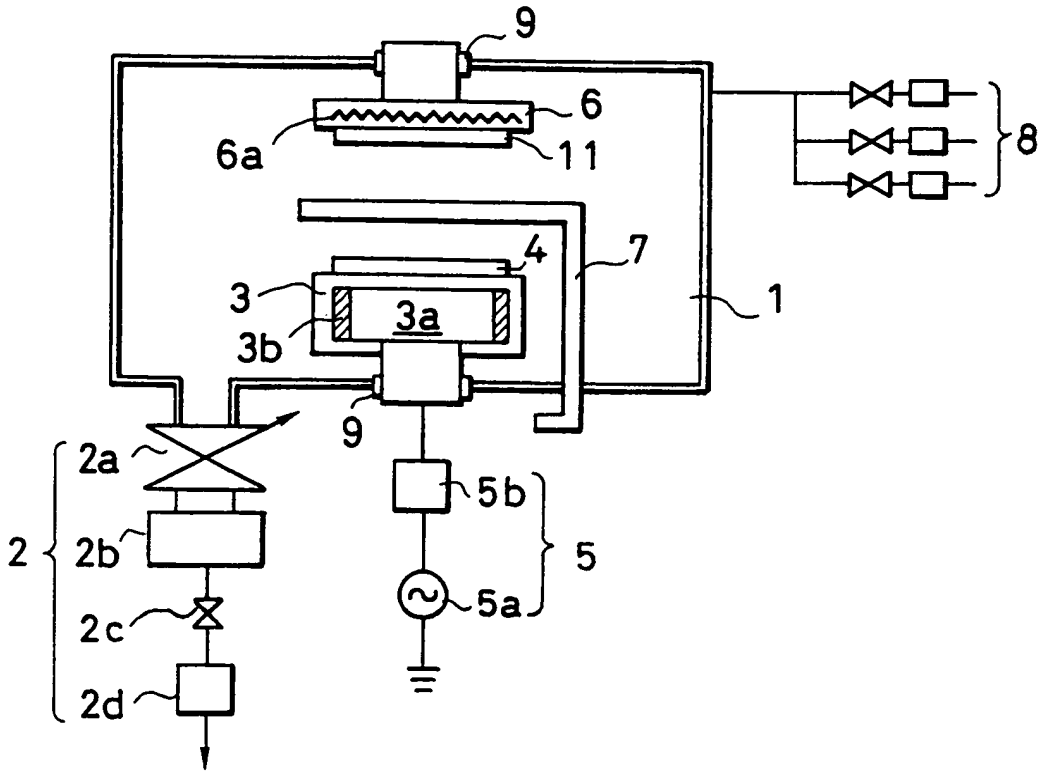

FIG. 1(B)

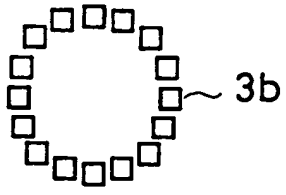

FIG. 2 (A)

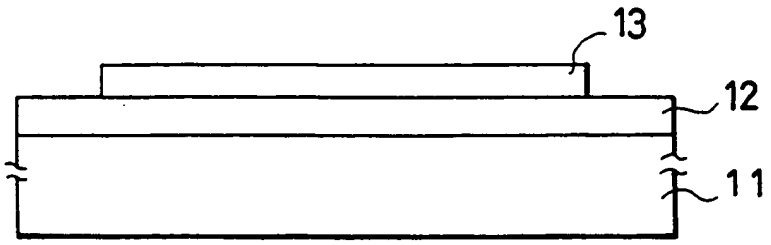

FIG. 2 (B)

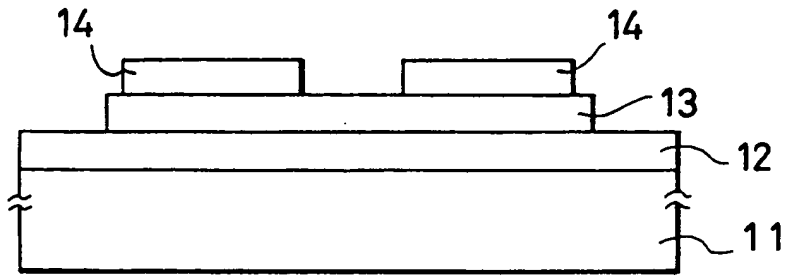

FIG. 2 (C)

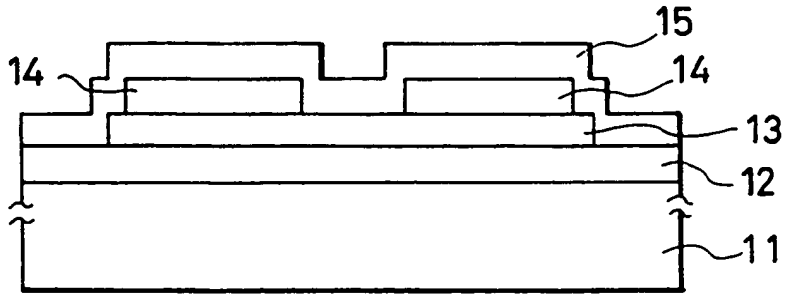

FIG. 2 (D)

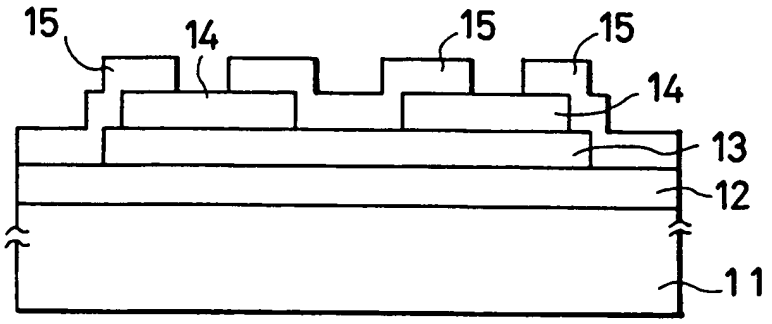

FIG. 2 (E)

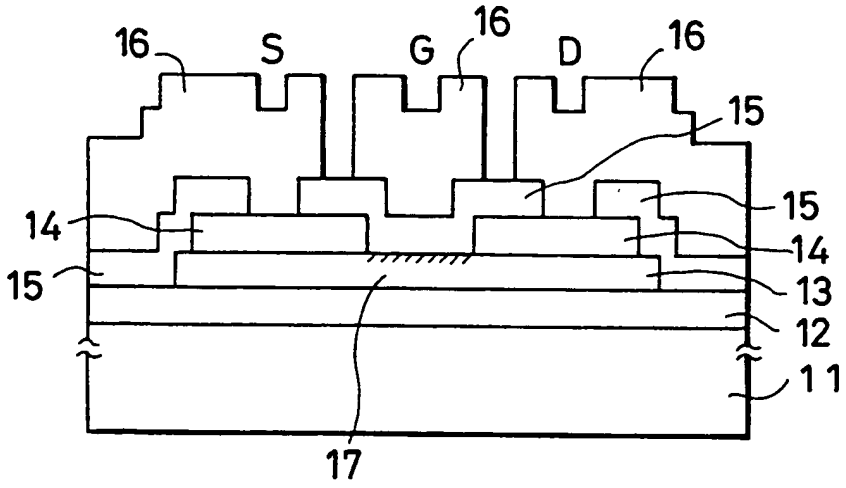

FIG. 3 (A)

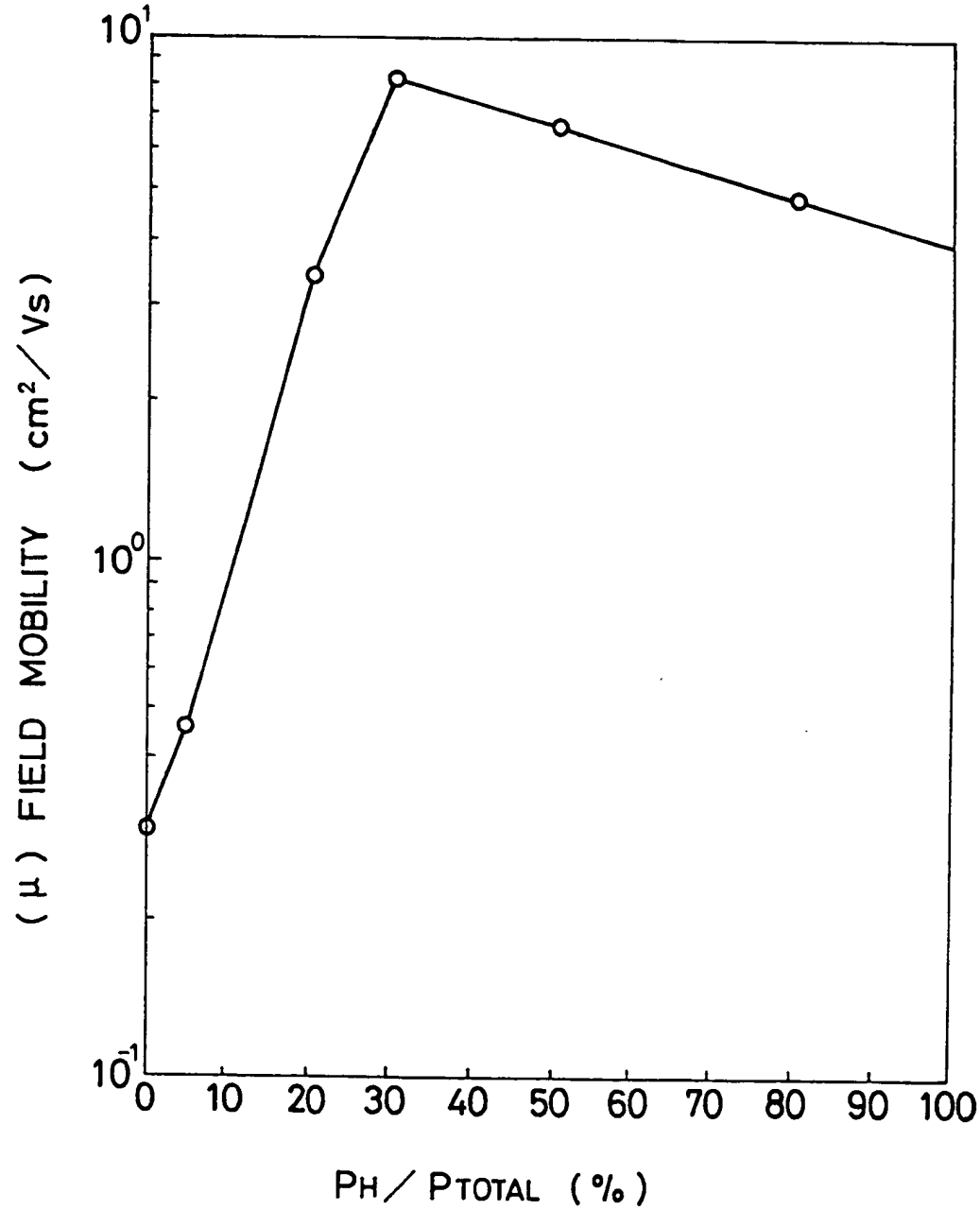
10^1
10^0
10^{-1}
(μ) FIELD MOBILITY (cm²/Vs)
0
10
20
30
40
50
60
70
80
90
100
PH / PTOTAL (%)

FIG. 3 (B)

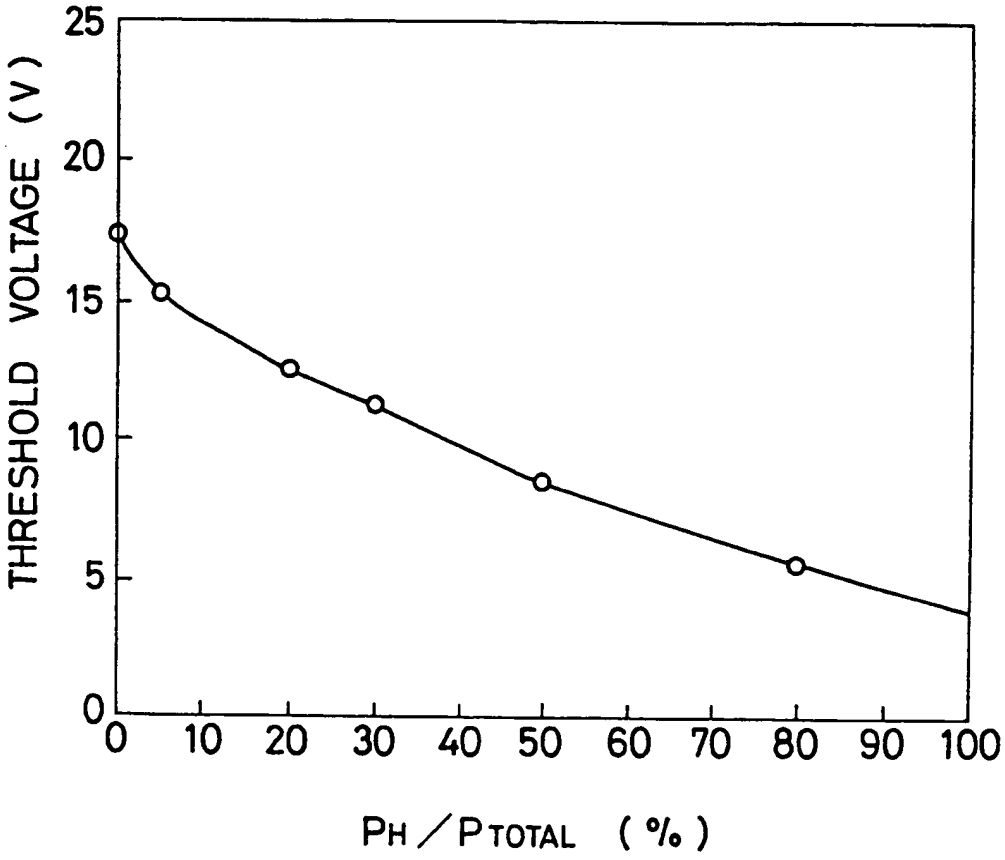
THRESHOLD VOLTAGE (V)
25
20
15
10
5
0
0
10
20
30
40
50
60
70
80
90
100
PH / PTOTAL (%)

FIG. 4

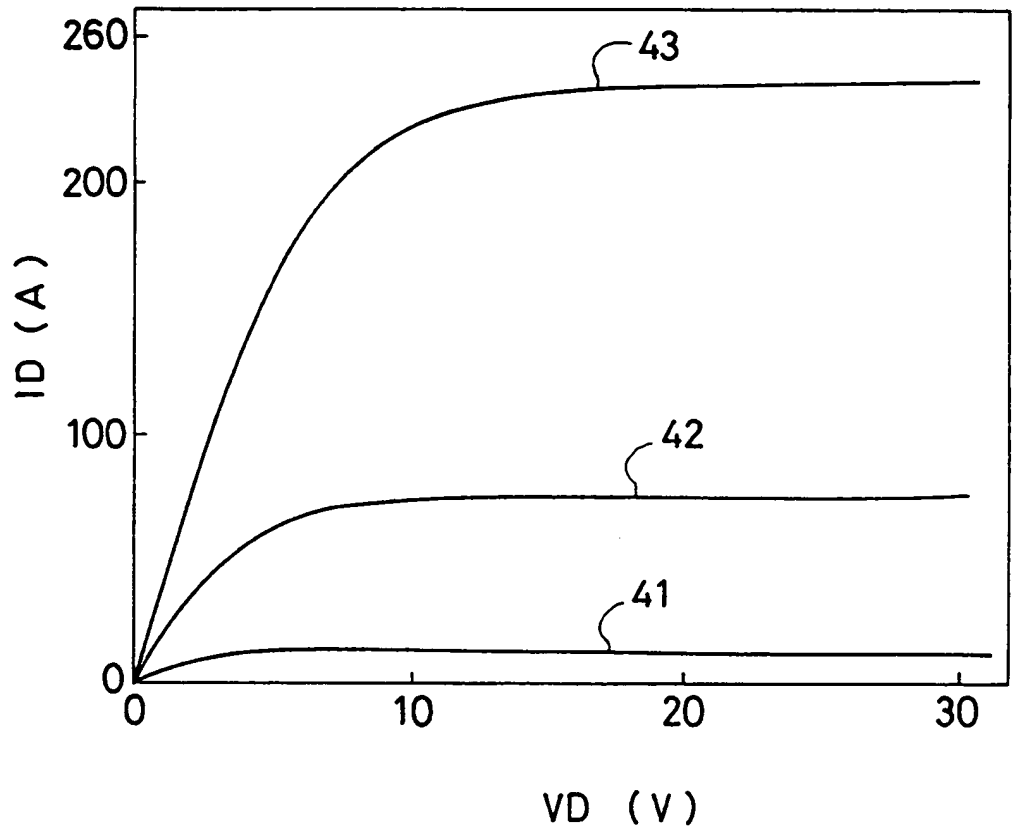

FIG. 5

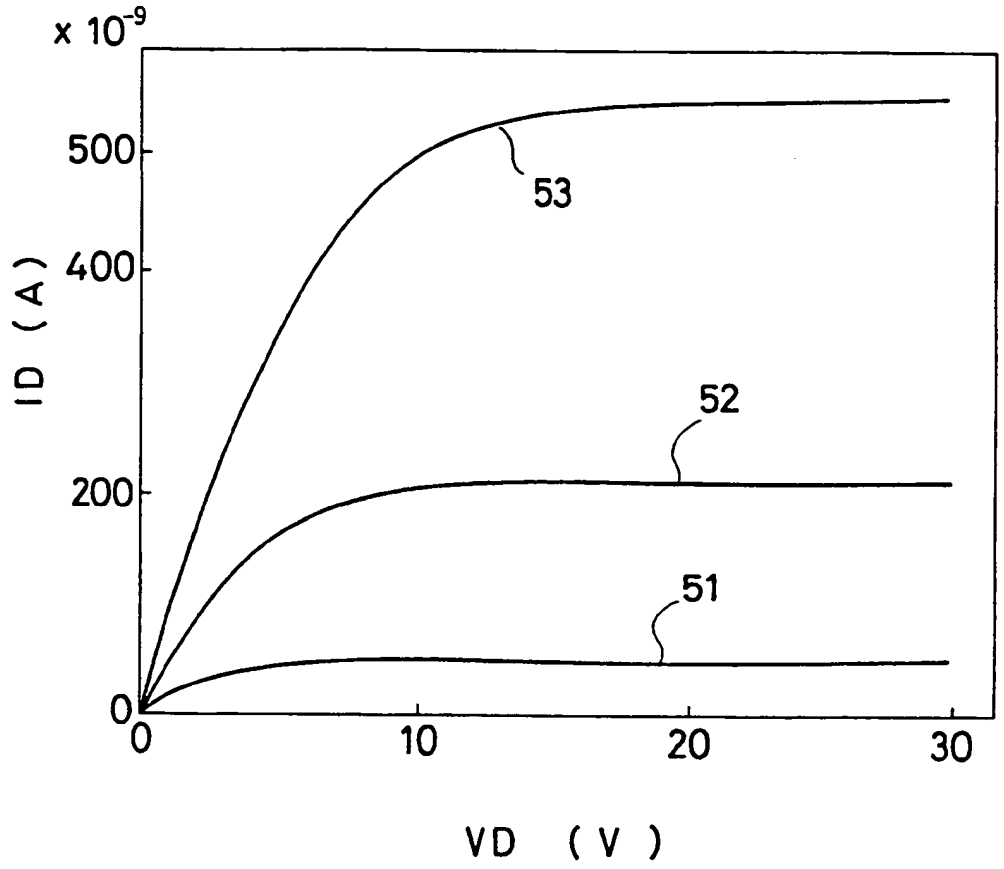

FIG. 6

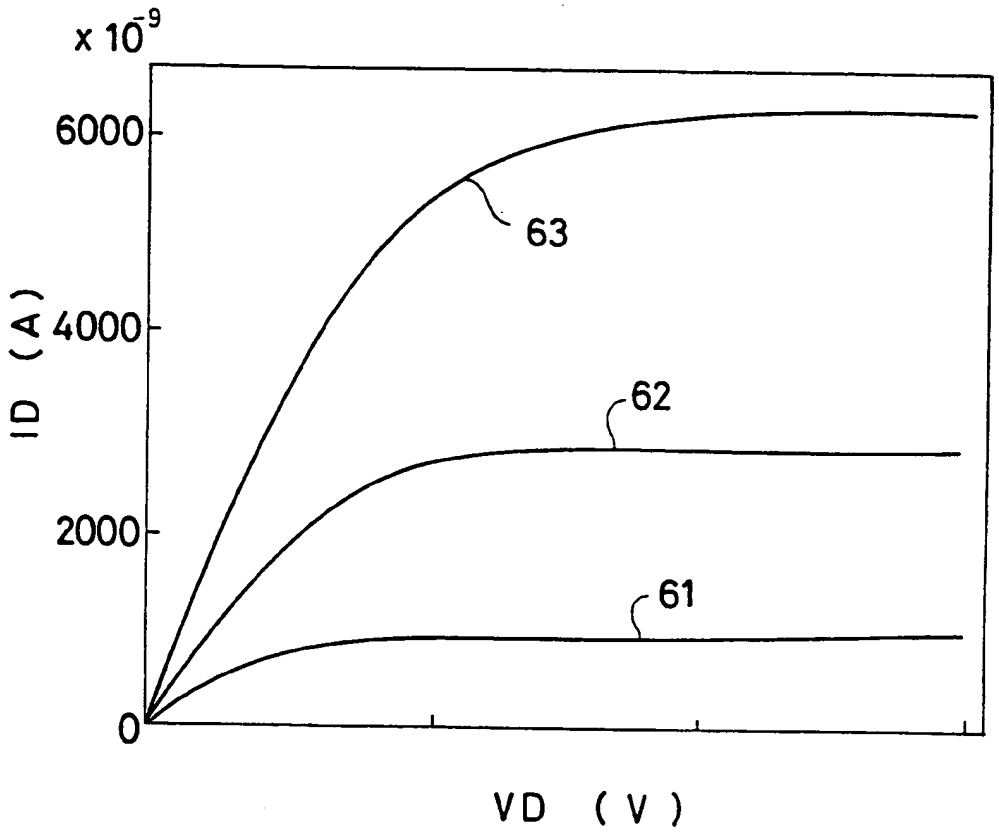

FIG. 7

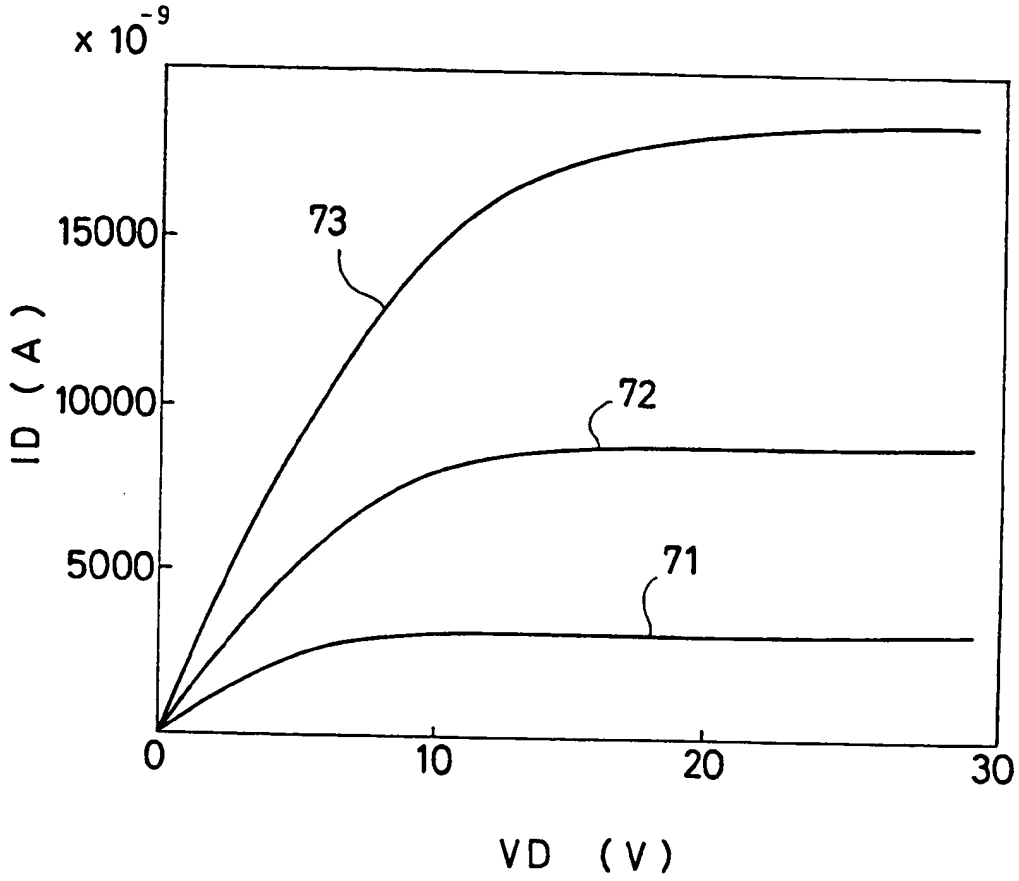

FIG. 8

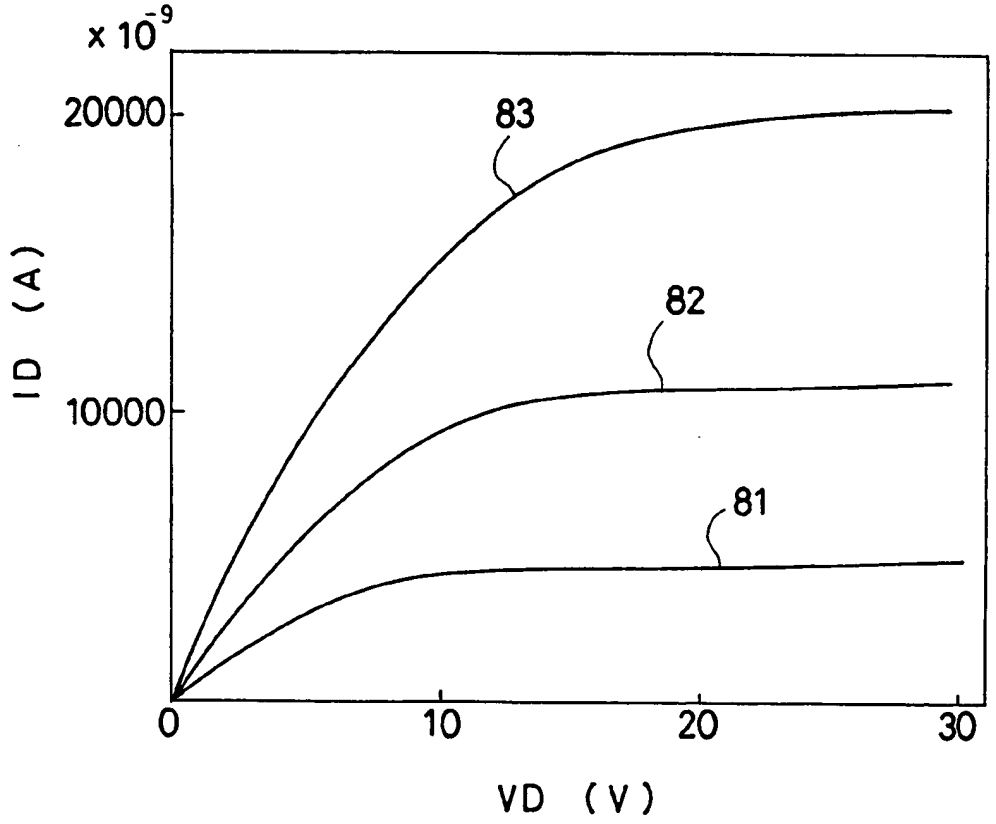

FIG. 9

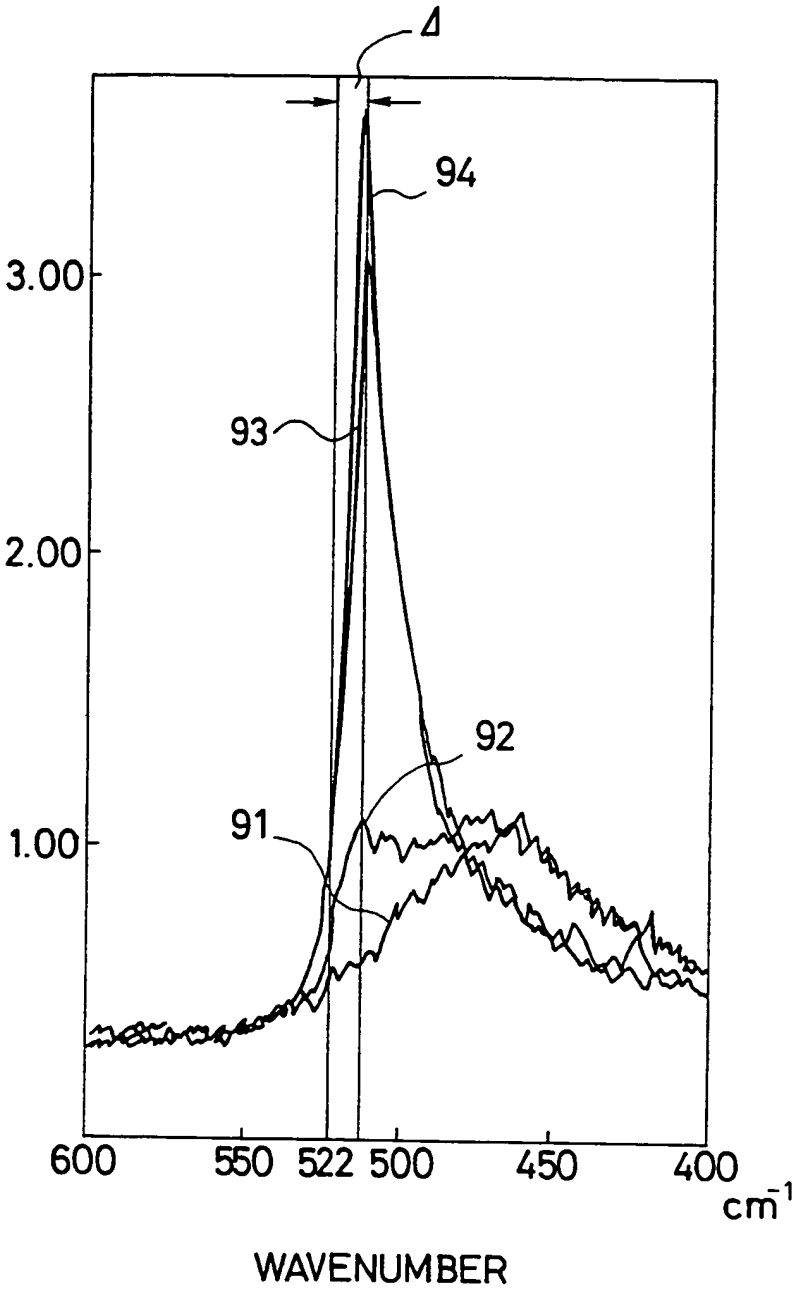

FIG. 10 (A)

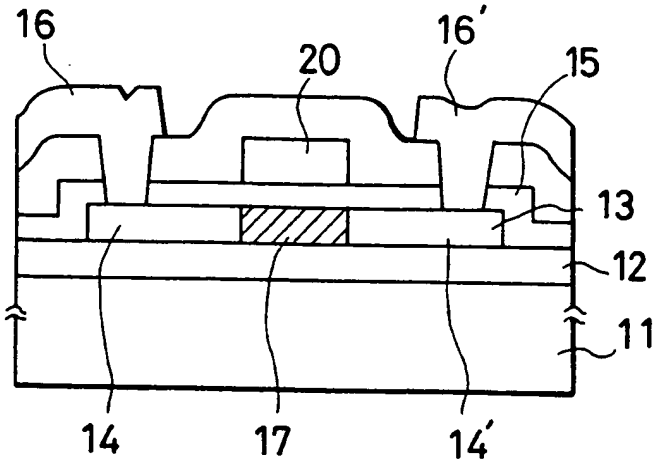

FIG. 10 (B)